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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,035	03/26/2004	Albert S. Weiner	ATM-291	8458
3897	7590	03/17/2006	EXAMINER	
SCHNECK & SCHNECK P.O. BOX 2-E SAN JOSE, CA 95109-0005			NGUYEN, THINH T	
			ART UNIT	PAPER NUMBER
			2818	
DATE MAILED: 03/17/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/810,035

Applicant(s)

WEINER, ALBERT S.

Examiner

Thinh T. Nguyen

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 20-30 is/are pending in the application.
- 4a) Of the above claim(s) 20-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

ELECTION/RESTRICTION

1. Claims 1-10 , 20-30 are presented for examination including new additional claim 20-30.
2. Newly submitted claims 20-30 are directed to inventions that is independent or distinct from the invention originally claimed for the following reasons:

I/ Species I: claims 1-10 directed toward a transistor memory array with special technical features as recited in claim 1(i.e. the mask ROM with one memory state)

II/ Species II: claims 20-30 directed toward a transistor memory array with special technical features as recited in claim 20 (i.e. the mask ROM with two memory state).

Since the applicant has received an action on the merits for the originally presented Invention (Species I) , this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 20-30 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1. 142(b) and MPEP 821.03.

3. This is in response to Applicant's Amendment filed 2/28/2006.

Note that the figures and reference numbers referred to in this Office Action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Art Unit: 2818

4. Applicant's amendments to independent claims 1 and dependant claim 3 have necessitated new grounds of rejection for claims 1-10. See MPEP § 706.07(a).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1-6,9-10 are rejected under 35 U.S.C. §102(e) as being anticipated by Lee et al.
(U.S. Patent 6,687,154)

REGARDING CLAIM 1

Lee (in fig 7B, in fig 9) discloses a transistor memory array comprising: a first plurality of non-volatile user programmable (cell 70a fig 7B) memory transistors and a second plurality of mask programmed read-only memory transistors (column 13 lines 16-17 ,cell 70b fig 7B), the non-volatile memory transistors and the read-only memory transistors having the same area footprint within a single memory array (column 13 line 13-32).

Art Unit: 2818

Noted that Lee discloses a Mask ROM cell and a Flash cell (i.e. user programmable non-volatile cell) using the same process and by shorting the control gate and the floating gate of the Flash cell to make a Mask Rom cell, therefore the two cells inherently have the same footprint and the same area footprint.

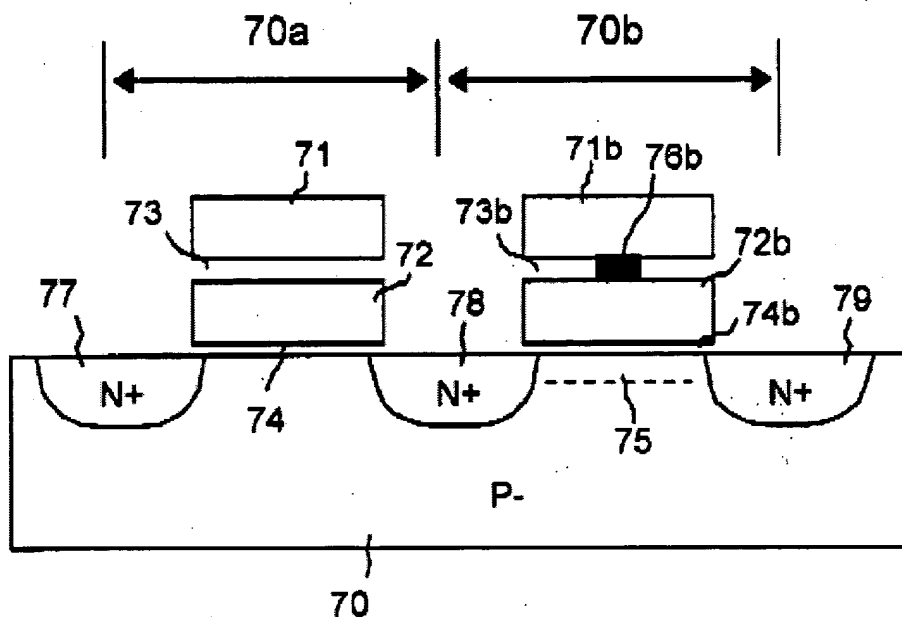


FIG. 7B

REGARDING CLAIM 2

Lee discloses (in column 6 lines 5) that the mask Rom cell can perform the select transistor function . and the rationale why the two cells have the same foot print has been discussed in the rejection of claim 1.

REGARDING CLAIM 3

Lee discloses (in fig 4,column 6 line 5) a memory array wherein the footprint has a longitudinal dimension and a width dimension that are the same for both the first and second pluralities of transistors. with the select transistor and memory transistor having a common electrode.

Noted that in fig 4 , the memory cell and the select transistor the control gate and gate are connected through lines 40a ,40b,40c,and 40d and therefore have common electrodes.

REGARDING CLAIM 4

Lee discloses (in column 13 lines 1-12) that the mask Rom cell can be closed or open using boron implantation (i.e. either the channel is not implanted by boron or implanted by boron dopant)

REGARDING CLAIM 5

Lee discloses (in column 12 lines 53-56,column 13 lines 25-36,fig 7A) a memory array wherein the no-volatile memory transistor have two poly layers and the ROM has only one poly layer

REGARDING CLAIM 6

Lee discloses (in fig 5) a memory array of claim 1 wherein the second plurality of read-only memory transistors is grouped into rows (row 50a and 50d in fig 5 are MASK ROM).

REGARDING CLAIM 9

Lee discloses (column 13 lines 1-12) a memory array wherein the channels in the read-only memory transistors are defined by a buried depletion implant in said substrate, the extent of the implant defining open and shorted channels.

REGARDING CLAIM 10

Lee discloses (in fig 9,column 6 line 37) a memory array wherein said non-volatile memory transistors are EEPROM transistors.

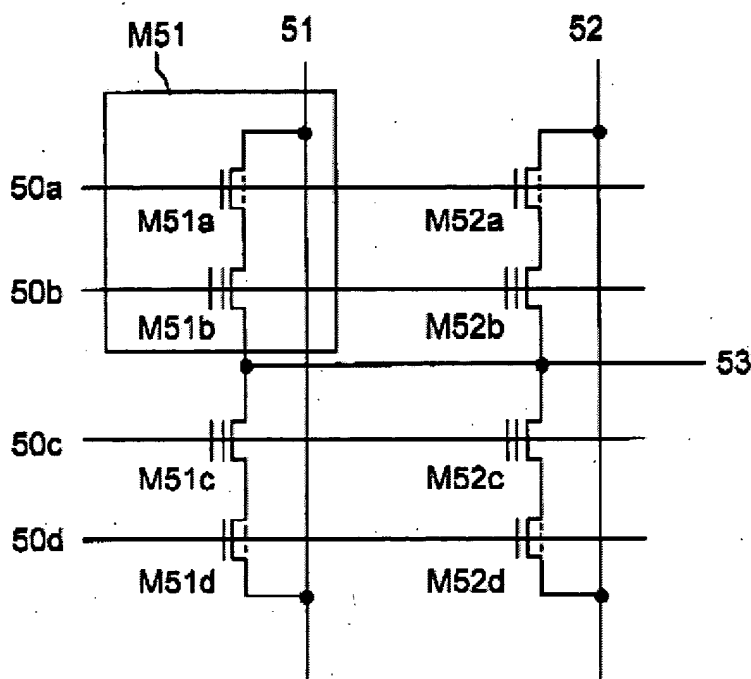


FIG. 5

Claim Rejections - 35 USC § 103

7. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art

Art Unit: 2818

are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negated by the manner in which the invention was made.

8. Claims 7,8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.
(U.S. patent 6,687,154)

REGARDING CLAIM 7,8.

With regard to claim 7,8 as set forth in the rejection of claim 6 , Lee discloses all the invention of claim 8 all the invention except for the condition of programming wherein the group of ROM cells has a first subgroup of transistors at least one row in first logic state and a second subgroup of transistors in at least one row second logic state.

It would have been obvious to one of ordinary skill in the art the time the invention was made to set the condition of programming wherein the group of ROM cells has a first subgroup of transistors at least one row in first logic state and a second subgroup of transistors in at least one row second logic state in the Lee device since it has been held that the provision of adjustability when needed ,involves only routine skill in the art (Noted that the adjustability skill in this case is a mere routine programming skill of a mask ROM (i.e. set one or set zero) during production to adjust to a particular application, also noted that Lee invention is highly flexible (column 13 lines 48-53) and can be applied to multiple applications(column 1 lines 27-40).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2818

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONCLUSION

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

Art Unit: 2818

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T Nguyen



Art Unit 2818



David Nelms
Supervisory Patent Examiner
Technology Center 2800